THE DESIGN OF LOW INDUCTANCE ELECTRICAL CIRCUITS FOR SLAPPER DETONATOR SYSTEMS

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ABSTRACT

Flying plate generators (FPG) are used to study the shock properties of various materials. This report investigates the theoretical electrical properties of the flat, parallel conductors that are currently used in the construction of FPGs. The design of these conductors can greatly effect the efficiency of FPGs by varying the high frequency capacitance and inductance of the electrical circuit, and the induced current in the surrounding system. The report derives rules governing the geometry of the conductors to minimise the inductance and capacitance of high frequency for such circuits.

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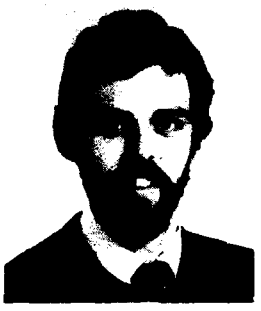

Ross Kummer obtained his BSc degree in Physics from the University of Melbourne in 1986. He obtained a Post-Graduate Diploma in Computing Science at La Trobe University in 1985 and in 1986 joined MRL. At MRL Ross has been involved with many aspects of computer modelling of explosive phenomenon and computer graphics. In 1989 he enrolled in a Masters Degree in Computer Science at La Trobe where he is currently studying a range of subjects such as image processing and knowledge bases systems.

CONTENTS

THE DESIGN OF LOW INDUCTANCE ELECTRICAL CIRCUITS FOR SLAPPER DETONATOR SYSTEMS

1. INTRODUCTION

In order to study and to model the effects of shock waves in materials and at interfaces, it is necessary to obtain parameters describing the materials' properties when subjected to high pressures. Of particular interest is the shock velocity of the material, and its relationship to the velocity of particles in the material.

The method we are looking at to obtain this data was developed by Steinberg and others [1]. It involves the use of the pressure wave from an electrically exploded metal foil to propel a thin sheet of plastic material to a very high velocity over a short distance. The flyer plate thus formed has well defined properties. Its impact with the material to be studied therefore provides a shock wave of precise pressure and time duration. From this, it is possible to measure the duration of the shock wave in the sample, as well as its velocity. Hence we can obtain accurate shock data on a range of materials.

The apparatus used, which is called a Flying Plate Generator, FPG [2] (a large scale slapper detonator-type device), is shown schematically in Figure 1. A voltage of several kilovolts is applied to the metal bridge foil (usually made from Aluminium or Copper). The bridge bursts in a very short time which depends mainly on its dimensions, and provides the pressure to form a flyer plate from the overlying plastic sheet. The tamper material beneath the bridge provides a reaction medium to improve the energy transfer efficiency to the plate. A spacer or barrel provides a stand-off distance between the bridge and the target or acceptor material, to enable the flyer plate to accelerate to near terminal velocity. The velocity achieved is a known function of the metal and the shape and size of the bridge foil used, the electrical circuit parameters, the plate material thickness and density, the barrel length (and diameter if small), and the thickness and density of the tamper. The FPG has been described in some detail elsewhere [2].

The burst behaviour of the bridge is central to correct functioning. We will now discuss the bridge burst behaviour, and the question of efficiency in some detail. Parts of the concept have been reported elsewhere [2, 14]. It has been found experimentally that the voltage across the bridge foil when it bursts forms a cusp-like curve, having a relatively low value until a time which is small relative to the time from the initial rise of current in the circuit. Beyond this point, the voltage rises approximately exponentially, and smoothly up to a maximum value, at which point the foil is considered to have burst. The time from initial rise of current to the point at which the bridge is burst, the peak in voltage across

the bridge, is defined as the burst time, t_b. At times greater than t_b, the voltage can behave in a number of different ways, depending on the circuit and foil designs. For the present purpose this is not important, since only the energy deposited in the bridge foil up to the burst time is important for efficiency in driving the flyer plate.

The physical mechanism by which the bridge bursts is not well known. In earlier work [9] we have given one view of the mechanism. Unlike the situation for exploding wires, there are no obvious discontinuities in the voltage characteristic which might correspond to phase changes in the foil as it transitions from a cold metal foil to an ionised vapour. This suggests that the foil goes directly to a vapour and ionises in a very short time in a combined sublimation-ionisation transition.

We have also found experimentally that the burst time t_b is not strongly dependent on the circuit characteristics, though it is dependent on the foil dimensions and capacitor charge voltage [15]. By altering the bridge dimensions we can vary the time at which a bridge will burst relative to the rise in current, for a fixed set of circuit parameters. Conversely, by varying the circuit parameters, we can alter the time at which the circuit current reaches its first maximum without significantly changing the foil burst time. Hence by this means we can experimentally adjust the bridge foil burst time relative to current maximum in order to obtain the highest efficiency.

We can maximise efficiency by the following argument. The power developed in the bridge foil is simply given by I^2R, for current I and bridge resistance R. Hence the total energy into the bridge is the time integral of this quantity. Since the resistance of the bridge has a similar characteristic to the voltage drop across the bridge (voltage changes much more rapidly than current during burst), the energy deposited into the bridge will only begin to rise rapidly when the resistance (or voltage) does. Hence it is only during the relatively small time immediately prior to the peak in voltage that significant energy is deposited into the foil, and hence that significant energy can be used to drive the flyer plate placed over the bridge. This energy can be maximised only by ensuring that the current is maximum at the burst time. Hence the system can be designed for maximum efficiency by ensuring that the bridge bursts at close to the first peak in current.

The efficiency for these systems may be defined as the ratio of the kinetic energy of the flyer plate to the energy initially stored on the capacitor,

$$\text{Efficiency} = (1/2\ mv_f^2)/(1/2\ CV^2)$$

Since it is only while the flyer plate is in close proximity to the bursting foil that it will obtain any acceleration from it, we assume that to obtain most efficient flyer plate acceleration, we must deposit the greatest amount of energy into the bridge foil at about the burst time t_b.

The time from initial rise in voltage across the bridge to its peak is very short (typically 5–50 ns depending on dimensions). Hence, up until the point where the bridge bursts, the resistance of the bridge may be considered small and constant. Therefore, until the burst point, (when a time-dependent resistance is introduced), the circuit behaves as a simple LRC circuit, with a frequency f given in terms of the (constant) inductance L, resistance R and capacitance C, by

$$\omega = 2\pi f = \sqrt{1/LC - (R/2L)^2} \qquad (1)$$

This equation assumes an underdamped circuit $((1/LC) > (R/2L)^2)$. The current in the circuit undergoes a damped sinusoidal oscillation.

For highest efficiency, the burst time should be close to the first peak in current, i.e. after one quarter period. Since the current is damped, the first peak is higher than subsequent ones. This optimisation can only be done with circuits which have very low inductance. The resistance and capacitance must also be kept low to keep eqn (1) valid and the period short. Since a capacitor is normally used to store the energy for the measurement, its value is not normally variable, 0.2 μF being a typical value in our present work. Resistance can be made very low by the use of short conductors, and low resistance components and connections.

The critical design parameter then becomes the circuit inductance, L, and we seek to obtain a value for it to ensure that bridge burst time t_b is close to the first current peak. This usually means that a very low value of inductance is necessary, though its specific value depends on the overall design, including capacitance used and the desired bridge/flyer plate dimensions. In this paper we discuss the question of how the inductance may be reduced to a small value, and present some design calculations to illustrate the problem. The obvious form of construction to use is called a "stripline", and it comprises two long and reasonably wide strips of metal foil separated by a thin (e.g. 25 μm thick) film of insulating material. This flat cable configuration has very low inductance, insignificant capacitance, and low resistance if the foil is kept thick enough.

In this paper, we describe calculations to estimate both capacitance and inductance of striplines. We have studied the effect of changes in the geometry of flat cable configurations, and give several useful results. In addition we have considered the inductance of several other conductor geometries which commonly occur in FPG designs. These include an examination of the effect of placing insulating "holes" in the stripline and the inductance of flat cables placed end-on. A study of the effects of metallic enclosures and clamps is also presented.

2. THE CALCULATIONS

2.1 Inductance

The method used is based on an analogy first recognised by Kelvin [4], used by Butterworth [5] and stated more clearly by Cockroft [6]. This states that at high enough frequency, the magnetic field lines become parallel to the surfaces of the conductors and thus do not penetrate them. This is due to the skin effect, and the current is concentrated on these surfaces. The distribution of magnetic fields due to the current density thus becomes analogous to the distribution of equipotential surfaces in an electrostatic problem, with magnetic field lines replacing equipotential surfaces, and the current density corresponding to the electrostatic surface charge density.

In the present work we assume that this high frequency limit applies. This suggests that there is only a small skin depth for the current into the conductors. We present in Table 1 a list of the skin depths as a function of frequency in copper. The skin depth is inversely proportional to the square root of the frequency. Table 1 shows that our assumption is reasonably valid for frequencies above a few hundred MHz. These are precisely the frequencies that the circuit experiences during a typical slapper detonator firing pulse.

(At low frequencies the current is distributed uniformly in the conductors and the present approach is not valid. Grover [7] has given a method, known as the 'Geometric Mean Distance' method for computing inductances in this case.) Inductance was estimated using a two-dimensional model of the stripline, and with the Boundary Element Method

[8,9]. The current distribution on the surfaces of a long stripline of the desired shape was calculated. From this the magnetic flux was calculated at points along a reference surface between the conductors, using the Biot-Savart Law. This was subsequently divided by the current in the system to give a value for the inductance per unit length [10].

Several geometric forms were studied. The first is shown in Figure 2. It represents a standard flat cable stripline. Both conductors have the same dimensions. We studied the effect on inductance of varying the width w, separation s and thickness t.

Because of the much smaller value of t compared with w, and even s in our case, (typical values are t = 18 μm, w = 20 mm, s = 50 μm), we experienced difficulties with the calculations, in that the lengths of Boundary Elements had to be highly variable around the surfaces. We were unable to keep all elements equal in length, though this is required for optimum accuracy [9]. Instead, we used only one or two elements along t, and varied the number of elements along w until the inductance estimate converged to a fixed value. The problem was thus treated as a sequence of estimates, with a limit to the sequence being estimated by assuming an arithmetico-geometric progression of the form [11]

$$\sum_{k=1}^{n-1} krq^k = \frac{(n-1)rq^n}{1-q} + \frac{rq(1-q^{n-1})}{(1-q)} \quad . \qquad (2)$$

The values of r and q were estimated from two points in the sequence (the first point was assumed to be the origin of the series). All points had to be evenly spaced in the incremental number of elements used. The values of r and q were then used to obtain the limiting value

$$\sum_{k=1}^{\infty} krq^k = \frac{rq}{(1-q)} \quad . \qquad (3)$$

Such an extrapolation gave good agreement with several more accurate calculations which we made.

2.1.1 Striplines

The results obtained are given in Table 2 for a range of w, s and t. Figures 3 and 4 show the dependence of inductance on width and separation. We found, as shown in Table 2, that inductance was not dependent on thickness of conductor for the thicknesses studied. We would expect inductance to increase for much thicker conductors, as edge effects will become more significant.

Figure 3 shows that the inductance depends strongly on conductor width, and is linear in the inverse of the width. We conclude from this that the width should be made large for low inductance. For a 10 mm wide stripline (t = 25 μm, s = 100 μm) the inductance of a 100 mm long stripline will be about 1 nH. The error in our calculation is estimated to be 10%.

Figure 4 shows that the effect of increasing separation of the conductors is to give a linear increase in inductance. Thus the separation of the conductors should be made as small as possible, commensurate with the dielectric strength of the insulator between them.

Simple application of the Biot-Savart Law to flat parallel conductors, neglecting conductor thickness and edge effects (Ryan and others [14]), gives an estimate for the inductance per unit length as

$$L = \mu_o \, s/w. \qquad (4)$$

where $\mu_o = 4\pi \times 10^{-7}$ is the permittivity of free space. In the limit of thin conductors of large width, eqn (4) should give results in agreement with our more detailed calculations.

Table 2 also shows the inductance per unit length calculated from the simple model of eqn (4). This model ignores conductor thickness and edge effects, and both these effects must account for at least some of the discrepancy between eqn (4) and the detailed calculations. It is difficult to estimate the magnitude of these effects relative to the error induced by the extrapolation procedure of eqn (2), Section 2.1. This error may be at least as large as edge and conductor thickness effects.

2.1.2 Holes

We have also looked at estimating the inductance of the configuration of conductors shown in Figure 5. This represents the case where the bridge is placed over a hole in the return conductor. (A hole permits a tamping plug to be inserted under the bridge.) Such a geometry was found to be much more difficult to treat accurately. We used similar methods to those for Fig 2, using eqns (2) and (3) to obtain the final value.

We found that for

w_b = 0.25 mm
t_b = 5 μm
s = 80 μm
w = 10 mm
t = 20 μm
g = 10 mm,

the inductance per unit length was about 1.8 μH/m, or nearly three orders of magnitude larger than that found from Fig. 2. (The calculation was done with 50 x 1 elements on the bridge and 500 x 1 elements on each part of the lower conductor.) Thus, despite the fact that regions having Fig. 5 geometry will generally be short, their contribution to total circuit inductance is expected to be significant.

To study the effect of the hole itself, we repeated the calculation with the hole region replaced by conducting material. That is, the gap shown in Fig 5 was removed and the two sections of lower conductor were replaced by a single conductor of the same length. With 50 x 1 elements on the bridge and 1000 x 1 elements on the lower conductor, we found a total inductance of 1.5 μH/m. Thus the hole itself contributes about 20% of the inductance in the bridge region.

Hence the region where the bridge lies over the lower stripline conductor should be kept as short as possible, and it is also advisable to avoid placing a hole in the lower stripline beneath the bridge.

2.1.3 End-on Conductors

The effect of placing two flat conductors end-on, as shown in Figure 6 has also been studied. The results of our calculations of inductance per unit length for the geometry shown in Figure 6, are given in Table 3. The parametric behaviour is shown in Figure 7 where we illustrate the effects of the width, thickness and separation of conductors on the inductance.

The trends of our results are similar to those with parallel plate conductors, as expected. As can be seen from Figure 7, the effect of increasing conductor width and thickness is to reduce inductance while increasing separation increases inductance. This can be understood from the expected behaviour of the magnetic field lines in each case. Decreasing width makes the conductors more like round wires. This has the same effect as decreasing the thickness, since in both cases, the edge effects become more significant, that is, the region between the conductors in which the magnetic field is uniform is reduced. Increasing separation between conductors allows more cross-sectional area for magnetic field lines, thereby increasing the flux in that region, and hence increasing the inductance.

Because of the importance of conductor thickness for this geometry, eqn (4) is not applicable in this case, and we must rely solely on the detailed calculations.

Note the scaling behaviour evident in the Table. If all dimensions are increased by the same amount, eg from w = 25 mm, s = 10 μm, t = 3 μm to w = 100 mm, s = 40 μm, t = 12 μm the inductance remains the same. This is to be expected since the current density in the conductors will reduce by the same amount as the increase in the linear dimension, leaving the magnetic flux reduced proportionately, and the integral of the flux over the area between conductors unchanged.

2.1.4 Clamps

We have examined the effects of placing metal clamps and blocks close to the stripline. The two forms modelled are shown in Figure 8. One consists of a block placed close to the stripline, while the other is a clamp which surrounds the stripline. Our calculations give the results shown in Table 4. We find that the clamps have little effect on the inductance of the striplines, even when placed close to them. As Figure 9 shows, however, they do have considerable eddy currents induced in them. The magnitude of the induced current is directly related to the spacing between stripline and clamp, being largest at the closest separation. The direction of the current induced in the clamp is always in the opposite direction to that in the adjacent stripline conductor.

These results suggest that the use of metal clamps should be avoided unless the insulation between them and the stripline is much thicker than the separation between the stripline conductors themselves. These calculations produce similar results to work reported elsewhere [10,12].

2.2 Experimental Results

Because of the very low inductances generally involved in the striplines, direct measurement at high frequency is very difficult. The simplest method we used was to estimate inductance from the current characteristic when a slapper detonator-type circuit was functioned with the slapper bridge replaced by a short circuit. Such a 'ringdown' procedure produces a ringing current, i.e. a damped sinusoidal characteristic in the ideal

case of constant switch resistance [3]. The total circuit inductance can be estimated [3] from the properties of the ringdown curve, primarily its period, if the circuit capacitance is known.

This measured inductance includes not only the stripline inductance, but also any inductance due to the attached capacitor and switch. In our present design the inductance of the capacitor is greater than the other circuit elements, being in the range 10–20 nH. This tends to mask the stripline inductance which is typically less than one tenth of this value, for a 100 mm long stripline.

We have attempted to study stripline inductance effects by increasing the length of the stripline from 100 mm to 400 mm. This fourfold increase did not produce any measurable change in the ringdown measurement of inductance, within the error of about 1 nH. We infer from this that the actual stripline inductance is at least of similar magnitude to the value calculated from our present work. For similar reasons, we decided not to attempt a direct measurement of the effect of a hole under the bridge in the stripline. Instead we observed its effect on the threshold energy for the system required to initiate a secondary explosive. Our results indicated a significant increase in required energy when the hole was present. Since it is known that inductance directly affects the threshold energy to initiate high explosive, (HE), and that in general lower circuit inductance leads to lower thresholds (down to some low value of inductance, probably below 5 nH) [13], we conclude that holes are indeed not a desirable design feature, and we recommend that they be avoided where possible.

Although a rigorous study of the effects of clamps was not undertaken, we have not been able, in any of our work, to attribute any effect of clamps on threshold energies or inductance values. We have rarely placed our clamps closer than 75 μm to the stripline conductors and therefore assume, along with the calculated results, that this is an acceptable separation to cause negligible effect on circuit operation.

2.3 Capacitance

For most stripline geometries it is reasonable to make flat-plate approximations, i.e. that edge effects are negligible. The capacitance of a stripline of area A, and conductor separation s is thus simply

$$C = \frac{\kappa \epsilon_o A}{s} \qquad (5)$$

where κ is the dielectric constant of the insulator, and ϵ_o is the dielectric permittivity of free space (8.854×10^{-12} $C^2 J^{-1} m^{-1}$). Because of our neglect of edge effects, the plate thickness does not appear in eqn (5), and is assumed not to contribute.

As eqn (5) shows, capacitance will increase linearly with increases in either length or width of the stripline. It also increases hyperbolically with decreases in plate separation. These conclusions partly conflict with the requirements for minimum inductance discussed in section 2.1, and some design compromise is in principle necessary.

Using a dielectric constant of $\kappa = 3.5$ for Kapton, and values of w = 10 mm, s = 100 μm for the Fig 2 geometry, we find that a 100 mm long strip will have a capacitance of 0.3 nF. Compared with a typical storage capacitance of about 0.2 μF, such a contribution is negligible, and we believe we are therefore free to vary the geometry to reduce inductance. For short striplines we can ignore capacitive contributions.

Note that to make a more accurate estimate of the capacitance effects, the Boundary Integral Method as used here for inductance calculations, can also be used. In this case we could make use of the electrostatic form of the calculation, rather than the Butterworth analogue. Because the capacitances estimated by eqn (5) are much smaller than the other capacitances normally included in the stripline circuit, eqn (5) was taken as adequate for the present purpose.

3. CONCLUSIONS

We have made a theoretical study of the effects of stripline design on its inductance and capacitance. We have found that to minimise inductance, it is desirable to

(i) use wide striplines

(ii) have the conducting strips close together

(iii) keep the conducting strips reasonably thin, and

(iv) keep the stripline as short as possible.

This partly conflicts with the requirements to keep stripline capacitance low, where we should

(i) use narrow width striplines

(ii) increase separation between conductors, and

(iii) keep the stripline short.

Actual estimates of inductance and capacitance for the case shown in Fig 2 show that the capacitive contribution is three orders of magnitude smaller than the storage capacitor value, and hence for short striplines can be ignored relative to the inductance. Stripline design (including the storage capacitor and switch) should therefore concentrate on minimising inductance.

We have shown that the effect of placing a hole in the return stripline under the region of the bridge is to introduce significant inductance and should therefore be avoided where possible.

A study of the effects of metal clamps placed near or around the stripline shows that though they do not significantly affect the circuit inductance, they do have eddy currents induced in them. These eddy currents can be large if the separation between clamp and stripline is small. Therefore it is desirable to ensure a relatively thick layer of insulation is placed between clamps and striplines. A separation of greater than 75 μm is recommended for stripline conductor thicknesses of 25 μm and separations of 70 μm.

Finally, note that Figs 3 and 4 suggest the following relationship between inductance per unit length L, width w and separation s, for the geometry of Fig 2,

$$L = \lambda\,(s/w). \qquad (6)$$

The data given in Table 2 provide a mean value of <lambda> = 1.1 for s in μm, w in mm and L in nH/m. In fact, simple analysis of the Biot-Savart Equation in two dimensions shows that in SI units, $\lambda = \mu_0$, the permittivity of free space, $\mu_0 = 4\pi \times 10^{-7}$ H/m (see eqn (4), above). For L in nH/m, s in μm and w in mm, eqn (4) gives an accurate value of 1.26 for λ in eqn (6). The deviations we have found from this value are due to both edge effects and to the accuracy of our extrapolation method described in Section 2.1.

The data presented in this report, through both tables and figures, permits the detailed design of striplines, and a reasonably accurate estimate of overall circuit inductance for components with a range of geometries. Data has been provided for a range of parameter sizes.

4. ACKNOWLEDGEMENTS

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Table 1 **Showing the relationship between skin depth and frequency ω for an alternating current in copper**

ω (MHz)	Period (ns)	Skin depth (μm)
1	6280	167
10	628	53
100	63	17
1000	6	5

Table 2 **Calculated inductance for the stripline shown in Fig. 2, and for a range of widths 2, separations s, and thicknesses t**

w (mm)	s (μm)	t (μm)	Inductance, L (nH/m)	Eqn (4) (nH/m)	
5.0	100	25	23	25	Effect of width
7.5	100	25	15	17	
10	100	25	11	13	
15	100	25	7	8	
7.5	50	25	7	8	Effect of separation
7.5	100	25	15	17	
7.5	150	25	23	25	
7.5	100	25	15	17	Effect of thickness
7.5	100	50	15	17	
7.5	100	125	15	17	

Table 3 **Calculated inductance for the end-on configuration shown in Fig. 6, and for a range of widths w, separations s, and thicknesses t**

w (mm)	s (μm)	t (μm)	Inductance, L (nH/m)
25	10	3	530
50	10	3	460
25	20	3	670
50	20	3	570
25	10	6	460
50	10	6	410
25	20	6	600
50	20	6	530
100	40	12	530

Table 4 **Calculated inductance for flat parallel striplines in the presence of clamps, as shown in Figure 8**

Dimensions (mm)						Inductance, L
w	s	t	s_s	w_c	t_c	(nH/m)
Block clamp						
7.5	0.025	0.025	0.025	12.5	10.0	6.7
7.5	0.025	0.025	0.05	12.5	10.0	6.7
7.5	0.025	0.025	0.1	12.5	10.0	6.7
Surround clamp						
7.5	0.05	0.025	0.025	12.5	0.15	6.7
7.5	0.05	0.025	0.05	12.5	0.2	6.7
7.5	0.05	0.025	0.1	12.5	0.3	6.7

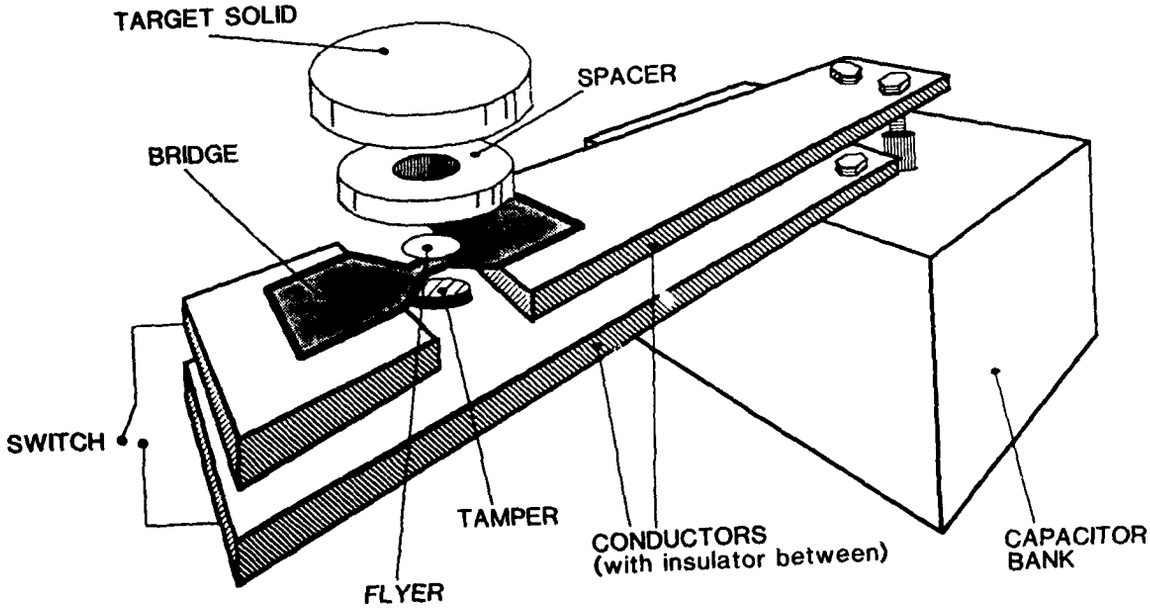

FIGURE 1 Exploded view of the apparatus for studying shock waves in materials.

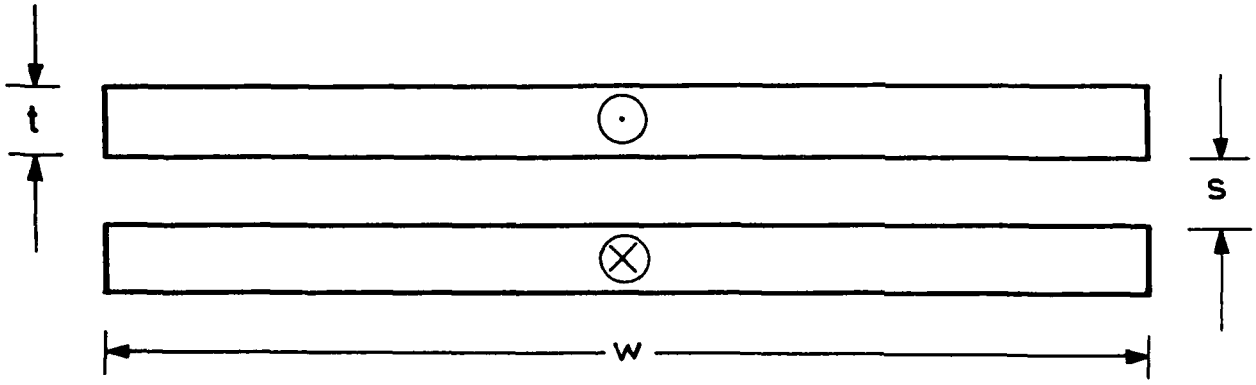

FIGURE 2 Schematic diagram of a flat cable stripline geometry.

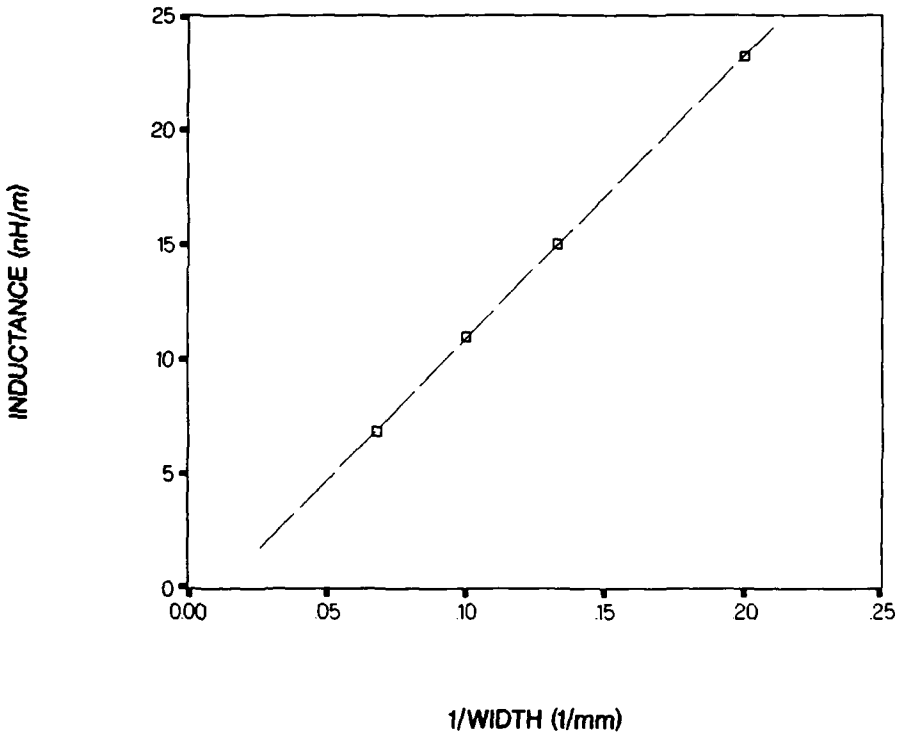

FIGURE 3 Showing the linear relationship between inductance and inverse width of the stripline drawn in Fig. 2.

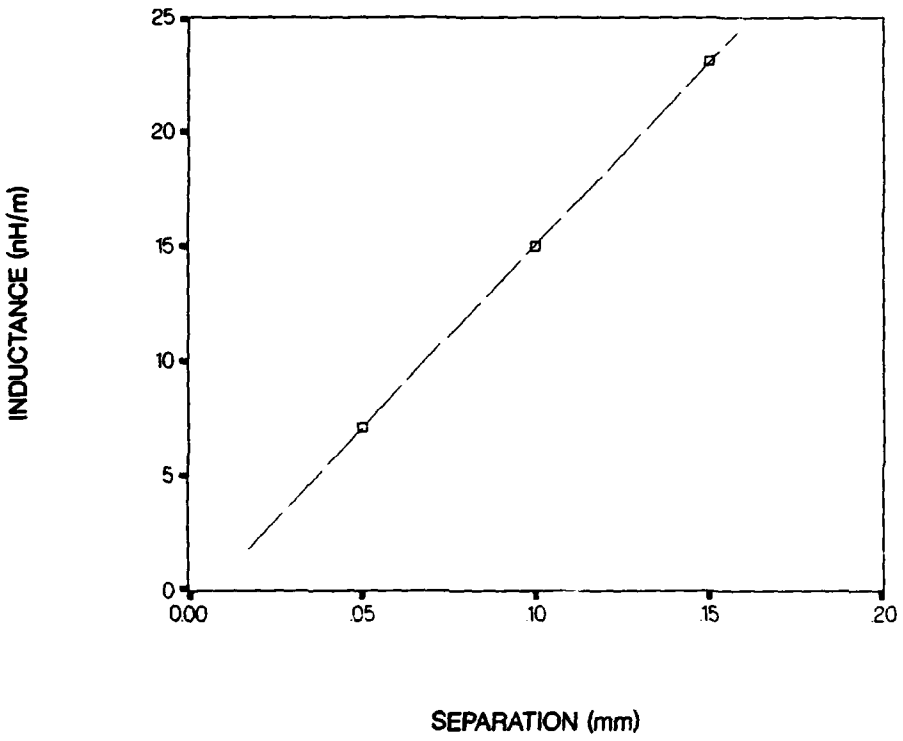

FIGURE 4 Showing the linear relationship between inductance and separation of the stripline shown in Fig. 2.

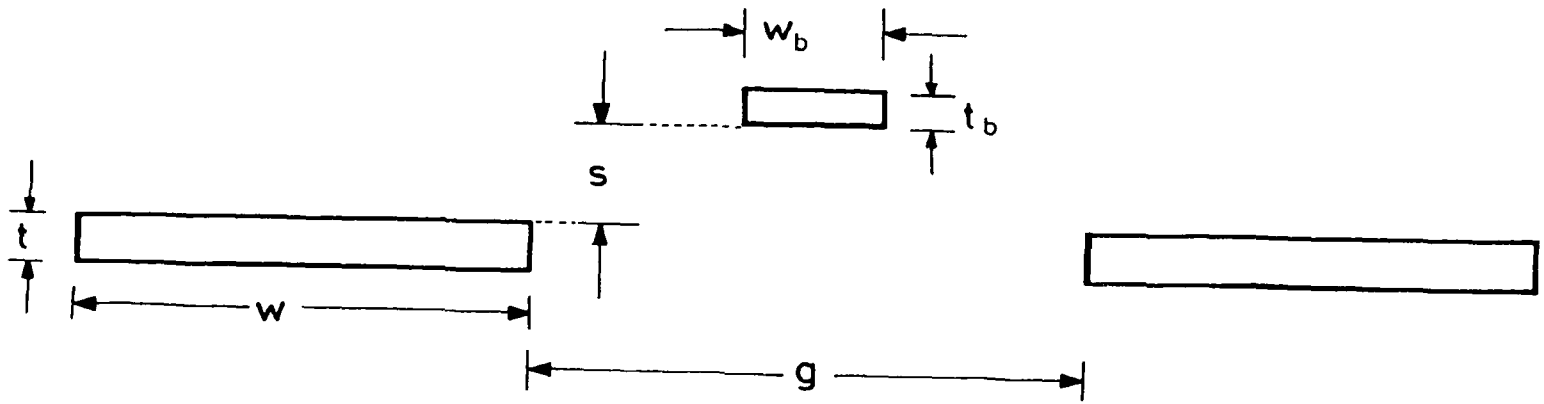

FIGURE 5 Schematic diagram of a stripline, studying the effect of placing the bridge over a whole in the return conductor.

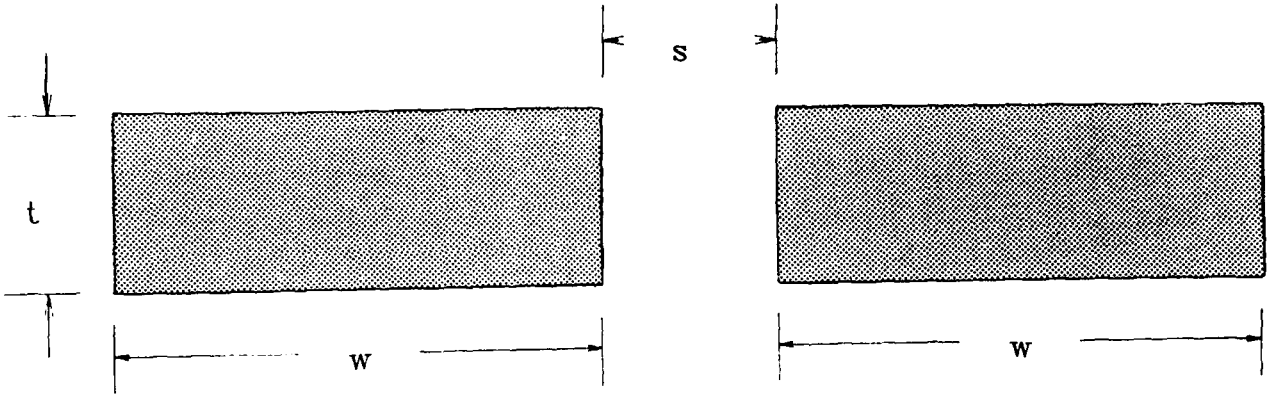

FIGURE 6 The geometric arrangement for two end-on conductors.

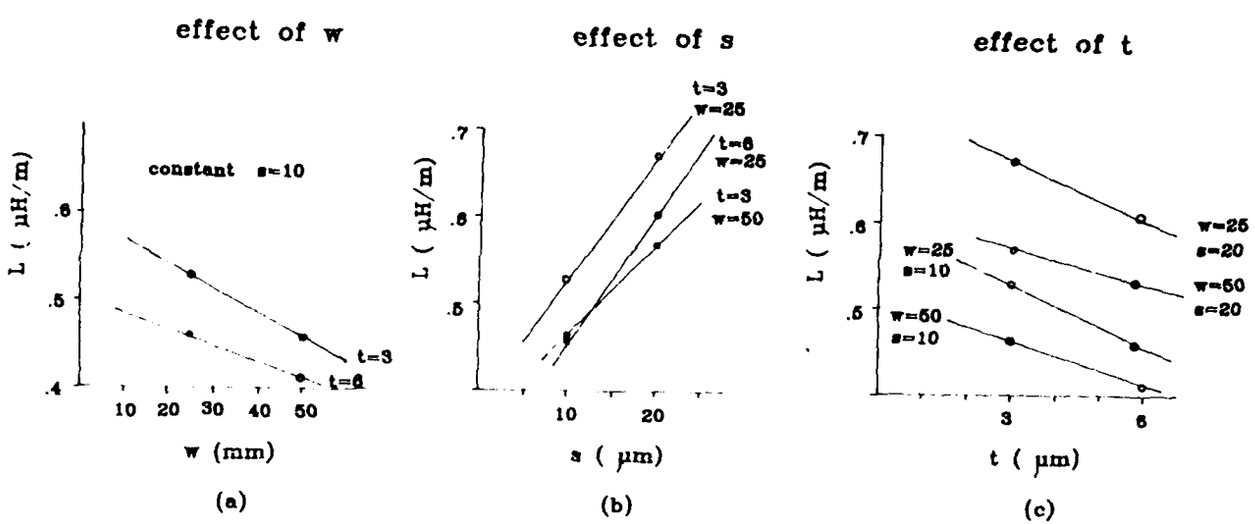

FIGURE 7 The effects on inductance per unit length of changes in the width, separation and thickness of the conductors on the end-on configuration of Figure 6.

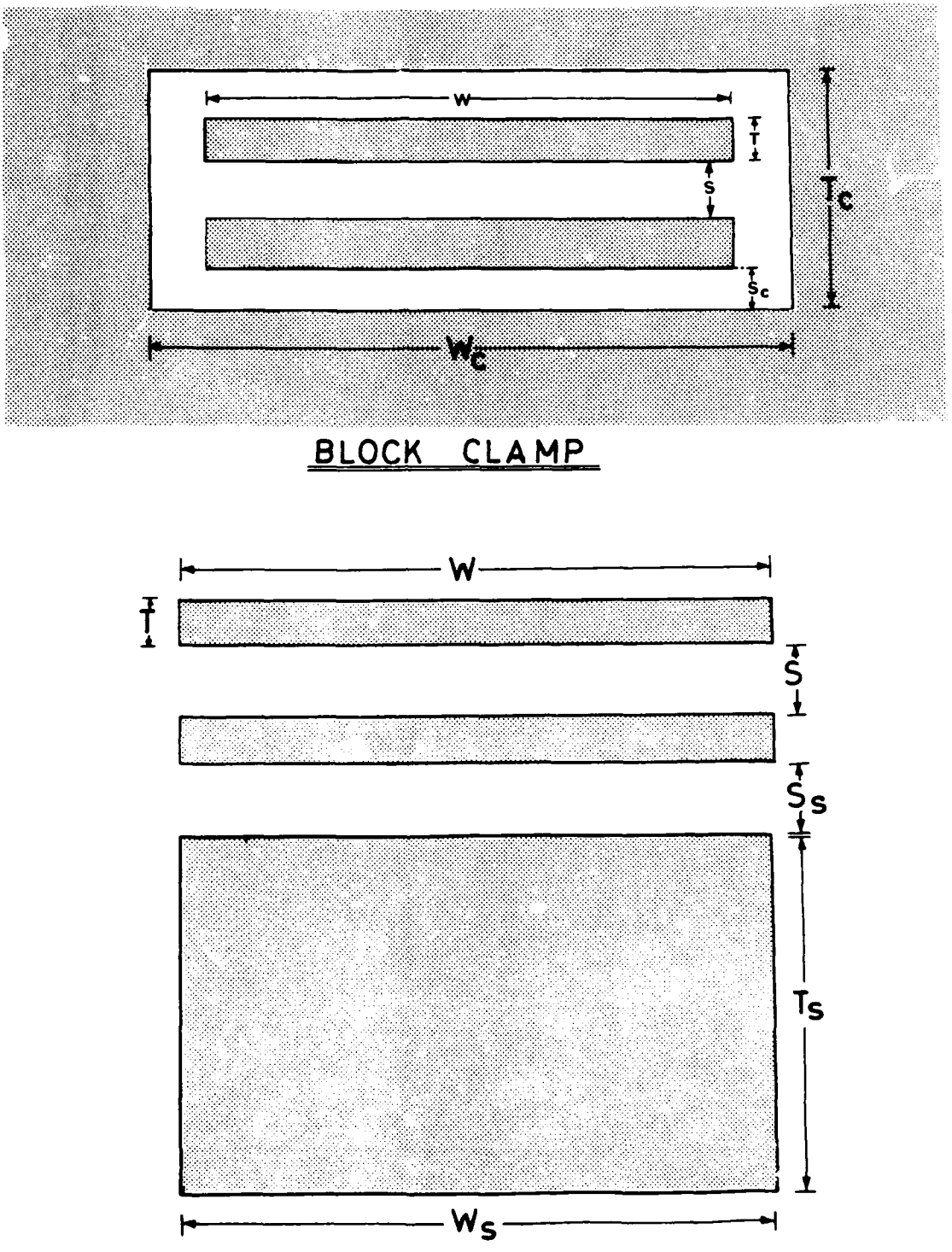

FIGURE 8 The clamp arrangements, showing (a) block clamp, and (b) surround clamp.

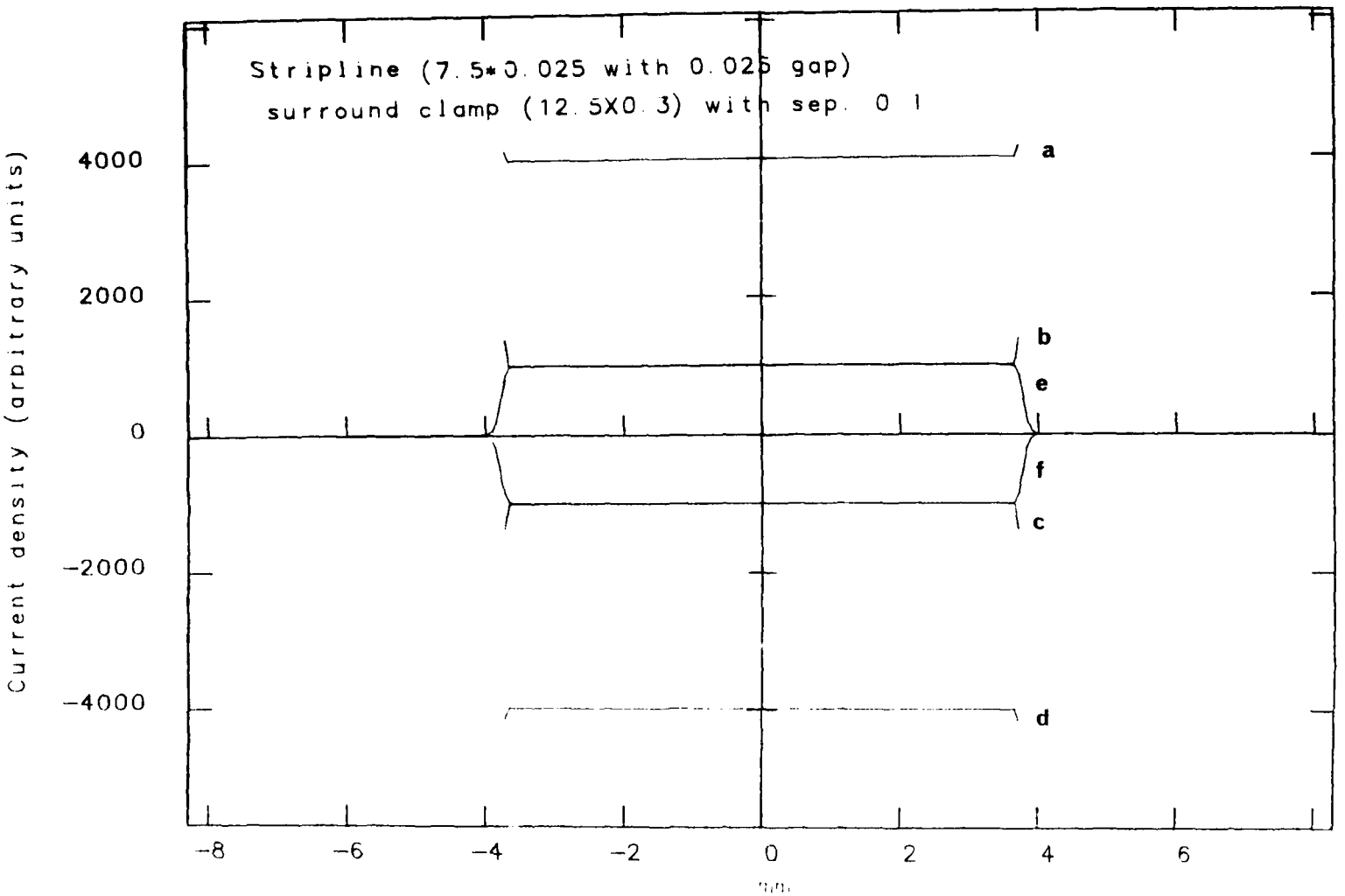

FIGURE 9(a) Showing current density on the surfaces of stripline conductors (a, b, c, d), and on the inner surfaces of a surrounding metal clamp (e, f).

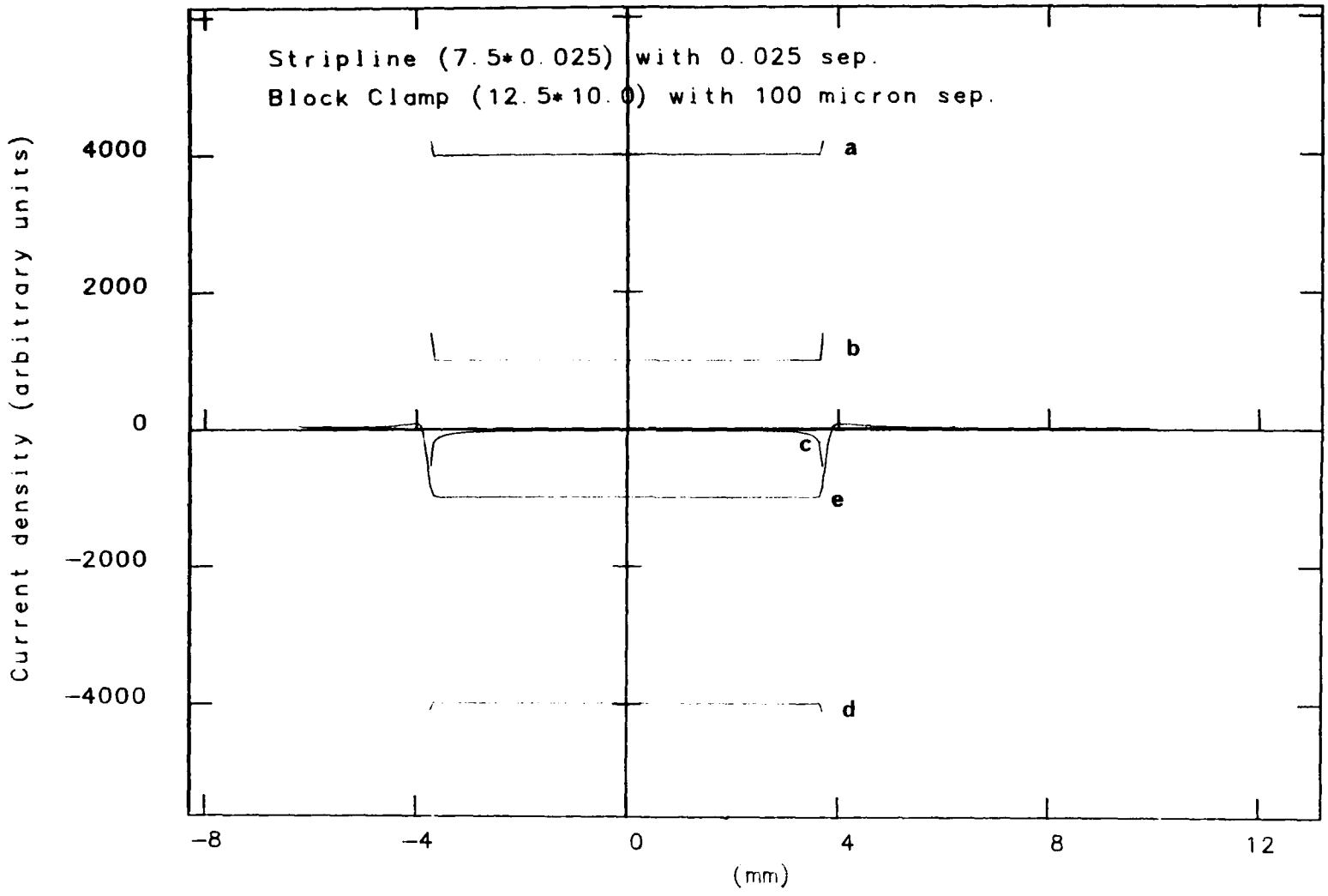

Figure 9(b) Showing current density on the surfaces of stripline conductors (a, b, c, d) and on the inner surface of a metal block placed nearby (e).

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The design of low inductance electrical circuits for slapper detonator systems

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ABSTRACT

Flying plate generators (FPG) are used to study the shock properties of various materials. This report investigates the theoretical electrical properties of the flat, parallel conductors that are currently used in the construction of FPGs. The design of these conductors can greatly effect the efficiency of FPGs by varying the high frequency capacitance and inductance of the electrical circuit, and the induced current in the surrounding system. The report derives rules governing the geometry of the conductors to minimise the inductance and capacitance of high frequency for such circuits.